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Case Docket No. PHD 99,046

THE COMMISSIONER OF PATENTS AND TRADEMARKS, Washington, D.C. 20231

Enclosed for filing is the patent application of Inventor(s):
 MAREIKE KLEE, RAINER KIEWITT, HANS-PETER LOBL, PAUL VAN OPPEN, ROBERT
 DERKSEN

For: VOLTAGE-DEPENDENT THIN-FILM CAPACITOR

ENCLOSED ARE:

- ☒ Associate Power of Attorney;
☐ Information Disclosure Statement, Form PTO-1449 and copies of documents listed therein;
☒ Preliminary Amendment;
☒ Specification (12 Pages of Specification, Claims, & Abstract);
☒ Declaration and Power of Attorney:
 (2 Pages of a ☐ fully executed ☒ unsigned Declaration);
☒ Drawing (2 sheets of ☐ informal ☒ formal sheets);
☒ Certified copy of GERMAN application Serial No. 19915247.0;
☒ Other: CITATION OF RELATED CASES;
☐ Assignment to .

FEE COMPUTATION

CLAIMS AS FILED				
FOR	NUMBER FILED	NUMBER EXTRA	RATE	BASIC FEE - 690.00
Total Claims	12 - 20 =	0	X \$18 =	0.00
Independent Claims	5 - 3 =	2	X \$78 =	156.00
Multiple Dependent Claims, if any			\$260 =	0.00
TOTAL FILING FEE				\$846.00

Please charge Deposit Account No. 14-1270 in the amount of the total filing fee indicated above, plus any deficiencies. The Commissioner is also hereby authorized to charge any other fees which may be required, except the issue fee, or credit any overpayment to Account No. 14-1270.

☐ Amend the specification by inserting before the first line the sentence: --This is a continuation-in-part of application Serial No. , filed .--.

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of

Atty. Docket

MAREIKE KLEE ET AL

PHD 99,046

Serial No.

Group Art Unit

Filed: CONCURRENTLY

Ex.

VOLTAGE-DEPENDENT THIN-FILM CAPACITOR

Honorable Commissioner of Patents and Trademarks
Washington, D.C. 20231

PRELIMINARY AMENDMENT

Sir:

Prior to examination please amend the above-identified case as follows:

IN THE SPECIFICATION

Page 1, before line 1, insert the following centered heading

--BACKGROUND OF THE INVENTION--.

between lines 21 and 22, insert the following centered heading

--SUMMARY OF THE INVENTION--;

Page 4, between lines 9 and 12, insert the following centered heading:

--BRIEF DESCRIPTION OF THE DRAWING--.

cancel lines 12 and 13 in their entirety and replace with a new paragraph:

--In the drawing--;

between lines 22 and 23, insert the following centered heading:

--DETAILED DESCRIPTION OF THE INVENTION--;

between lines 23 and 23, insert as a new paragraph:

--The invention will now be described in greater detail with reference to the figures of the drawing.--.

IN THE ABSTRACT

Please delete in its entirety and replace with the following:

12272 12273 12274 12275 12276 12277 12278 12279 12280 12281 12282 12283 12284 12285 12286 12287 12288 12289 12290 12291 12292 12293 12294 12295 12296 12297 12298 12299 12300 12301 12302 12303 12304 12305 12306 12307 12308 12309 12310 12311 12312 12313 12314 12315 12316 12317 12318 12319 12320 12321 12322 12323 12324 12325 12326 12327 12328 12329 12330 12331 12332 12333 12334 12335 12336 12337 12338 12339 12340 12341 12342 12343 12344 12345 12346 12347 12348 12349 12350 12351 12352 12353 12354 12355 12356 12357 12358 12359 12360 12361 12362 12363 12364 12365 12366 12367 12368 12369 12370 12371 12372 12373 12374 12375 12376 12377 12378 12379 12380 12381 12382 12383 12384 12385 12386 12387 12388 12389 12390 12391 12392 12393 12394 12395 12396 12397 12398 12399 12400 12401 12402 12403 12404 12405 12406 12407 12408 12409 12410 12411 12412 12413 12414 12415 12416 12417 12418 12419 12420 12421 12422 12423 12424 12425 12426 12427 12428 12429 12430 12431 12432 12433 12434 12435 12436 12437 12438 12439 12440 12441 12442 12443 12444 12445 12446 12447 12448 12449 12450 12451 12452 12453 12454 12455 12456 12457 12458 12459 12460 12461 12462 12463 12464 12465 12466 12467 12468 12469 12470 12471 12472 12473 12474 12475 12476 12477 12478 12479 12480 12481 12482 12483 12484 12485 12486 12487 12488 12489 12490 12491 12492 12493 12494 12495 12496 12497 12498 12499 12500 12501 12502 12503 12504 12505 12506 12507 12508 12509 12510 12511 12512 12513 12514 12515 12516 12517 12518 12519 12520 12521 12522 12523 12524 12525 12526 12527 12528 12529 12530 12531 12532 12533 12534 12535 12536 12537 12538 12539 12540 12541 12542 12543 12544 12545 12546 12547 12548 12549 12550 12551 12552 12553 12554 12555 12556 12557 12558 12559 12560 12561 12562 12563 12564 12565 12566 12567 12568 12569 12570 12571 12572 12573 12574 12575 12576 12577 12578 12579 12580 12581 12582 12583 12584 12585 12586 12587 12588 12589 12590 12591 12592 12593 12594 12595 12596 12597 12598 12599 12600 12601 12602 12603 12604 12605 12606 12607 12608 12609 12610 12611 12612 12613 12614 12615 12616 12617 12618 12619 12620 12621 12622 12623 12624 12625 12626 12627 12628 12629 12630 12631 12632 12633 12634 12635 12636 12637 12638 12639 12640 12641 12642 12643 12644 12645 12646 12647 12648 12649 12650 12651 12652 12653 12654 12655 12656 12657 12658 12659 12660 12661 12662 12663 12664 12665 12666 12667 12668 12669 12670 12671 12672 12673 12674 12675 12676 12677 12678 12679 12680 12681 12682 12683 12684 12685 12686 12687 12688 12689 12690 12691 12692 12693 12694 12695 12696 12697 12698 12699 12700 12701 12702 12703 12704 12705 12706 12707 12708 12709 12710 12711 12712 12713 12714 12715 12716 12717 12718 12719 12720 12721 12722 12723 12724 12725 12726 12727 12728 12729 12730 12731 12732 12733 12734 12735 12736 12737 12738 12739 12740 12741 12742 12743 12744 12745 12746 12747 12748 12749 12750 12751 12752 12753 12754 12755 12756 12757 12758 12759 12760 12761 12762 12763 12764 12765 12766 12767 12768 12769 12770 12771 12772 12773 12774 12775 12776 12777 12778 12779 12780 12781 12782 12783 12784 12785 12786 12787 12788 12789 12790 12791 12792 12793 12794 12795 12796 12797 12798 12799 12800 12801 12802 12803 12804 12805 12806 12807 12808 12809 12810 12811 12812 12813 12814 12815 12816 12817 12818 12819 12820 12821 12822 12823 12824 12825 12826 12827 12828 12829 12830 12831 12832 12833 12834 12835 12836 12837 12838 12839 12840 12841 12842 12843 12844 12845 12846 12847 12848 12849 12850 12851 12852 12853 12854 12855 12856 12857 12858 12859 12860 12861 12862 12863 12864 12865 12866 12867 12868 12869 12870 12871 12872 12873 12874 12875 12876 12877 12878 12879 12880 12881 12882 12883 12884 12885 12886 12887 12888 12889 12890 12891 12892 12893 12894 12895 12896 12897 12898 12899 12900 12901 12902 12903 12904 12905 12906 12907 12908 12909 12910 12911 12912 12913 12914 12915 12916 12917 12918 12919 12920 12921 12922 12923 12924 12925 12926 12927 12928 12929 12930 12931 12932 12933 12934 12935 12936 12937 12938 12939 12940 12941 12942 12943 12944 12945 12946 12947 12948 12949 12950 12951 12952 12953

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 135. *Chlorophyll ee* (Chl *ee*)
 136. *Chlorophyll ef* (Chl *ef*)
 1

(b)

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Voltage-dependent thin-film capacitor.

The invention relates to a ceramic passive component which comprises a carrier substrate, at least a first electrode disposed thereon, at least a dielectric disposed thereon, and at least a second electrode disposed thereon. The invention also relates to components in which at least one ceramic passive component with the above construction is used.

5 Variable-capacitance diodes (also called varicaps) are diodes in which the voltage dependence of a pn junction is utilized in practice. Each pn junction forms a capacitor with the p- and the n-zone as the plates and the interposed depletion or blocking layer as the dielectric. The thickness of the depletion layer increases with the applied reverse voltage, so that the capacitance value of the pn junction decreases.

10 Variable-capacitance diodes are available in various embodiments. Typical operating voltages are 12 to 30 V accompanied by a capacitance which is variable by a factor 10 to 20. Lower voltages in a range from 3 to 5 V are usual in mobile telephone applications with a tuning range having a factor between 2 and 4. The capacitance values of the diodes usually vary between 20 and 40 pF in this case. These semiconductor components are used
15 inter alia in the manufacture of voltage-controlled oscillators (VCOs).

The present trend is towards lower voltages and high frequencies (GHz) especially in the field of mobile telephony. The construction of variable-capacitance diodes for this application, however, becomes increasingly difficult, especially if the dimensions of the components have to be as small as possible. The semiconductor components also come close
20 to the limits of their possibilities in view of their effective series resistance. In addition, the cost of manufacture of variable-capacitance diodes is very high.

The invention has for its object to provide a component which has a tunable capacitance as well as a low effective series resistance and which can be inexpensively manufactured.

25 This object is achieved by means of a ceramic passive component which comprises a carrier substrate, at least a first electrode disposed thereon, at least a dielectric disposed thereon, and at least a second electrode disposed thereon, wherein the dielectric comprises a ferroelectric ceramic material with a voltage-dependent relative dielectric constant ϵ_r .

Given certain geometric dimensions (surface area A , electrode spacing d), the capacitance of a capacitor can be calculated from the equation:

$$C = (\epsilon_r \cdot \epsilon_0 \cdot A)/d.$$

A voltage dependence of the capacitance C is thus defined by the voltage dependence of the dielectric constant ϵ_r . Many dielectric materials exhibit a low dielectric constant ϵ_r and a low field dependence $\epsilon_r(E)$. An exception is formed by ferroelectric materials, in which ϵ_r can be changed through the application of an electric field E . The capacitance value C of a capacitor can thus be changed through the application of a voltage to the electrodes.

The advantages of these components are that on the one hand they are not polar, in contrast to variable-capacitance diodes, and on the other hand that they can be manufactured more cheaply than the semiconductor components.

It is to be highly preferred that the following is chosen as the ferroelectric ceramic material with a voltage-dependent dielectric constant ϵ_r :

$\text{Pb}(\text{Zr}_x\text{Ti}_{1-x})\text{O}_3$ ($0 \leq x \leq 1$) with and without excess lead, $\text{Ba}_{1-x}\text{Sr}_x\text{TiO}_3$ ($0 \leq x \leq 1$),

$\text{Pb}_{1-1.5y}\text{La}_y(\text{Zr}_x\text{Ti}_{1-x})\text{O}_3$ ($0 \leq x \leq 1$, $0 \leq y \leq 0.2$), $\text{Pb}(\text{Zr}_x\text{Ti}_{1-x})\text{O}_3$ ($0 \leq x \leq 1$) doped with Nb, $\text{Pb}_{1-\alpha y}\text{La}_y\text{TiO}_3$ ($0 \leq y \leq 0.3$, $1.3 \leq \alpha \leq 1.5$), $(\text{Pb}, \text{Ca})\text{TiO}_3$, BaTiO_3 with and without dopants, $\text{SrZr}_x\text{Ti}_{1-x}\text{O}_3$ ($0 \leq x \leq 1$) with and without Mn dopants, $\text{BaZr}_x\text{Ti}_{1-x}\text{O}_3$ ($0 \leq x \leq 1$), SrTiO_3 doped with, for example, La, Nb, Fe or Mn,

$[\text{Pb}(\text{Mg}_{1/3}\text{Nb}_{2/3})\text{O}_3]_x[\text{PbTiO}_3]_{1-x}$ ($0 \leq x \leq 1$),

$(\text{Pb}, \text{Ba}, \text{Sr})(\text{Mg}_{1/3}\text{Nb}_{2/3})_x\text{Ti}_y(\text{Zn}_{1/3}\text{Nb}_{2/3})_{1-x-y}\text{O}_3$ ($0 \leq x \leq 1$, $0 \leq y \leq 1$, $x + y \leq 1$),

$\text{PbNb}_{4/5x}((\text{Zr}_{0.6}\text{Sn}_{0.4})_{1-y}\text{Ti}_y)_{1-x}\text{O}_3$ ($0 \leq x \leq 0.9$, $0 \leq y \leq 1$), $(\text{Ba}_{1-x}\text{Ca}_x)\text{TiO}_3$ ($0 \leq x \leq 1$),

$(\text{Ba}_{1-x}\text{Sr}_x)\text{TiO}_3$ ($0 \leq x \leq 1$), $(\text{Ba}_{1-x}\text{Pb}_x)\text{TiO}_3$ ($0 \leq x \leq 1$), $(\text{Ba}_{1-x}\text{Sr}_x)(\text{Ti}_{1-x}\text{Zr}_x)\text{O}_3$

($0 \leq x \leq 1$, $0 \leq y \leq 1$),

a) $\text{Pb}(\text{Mg}_{1/2}\text{W}_{1/2})\text{O}_3$

b) $\text{Pb}(\text{Fe}_{1/2}\text{Nb}_{1/2})\text{O}_3$

c) $\text{Pb}(\text{Fe}_{2/3}\text{W}_{1/3})\text{O}_3$

d) $\text{Pb}(\text{Ni}_{1/3}\text{Nb}_{2/3})\text{O}_3$

e) $\text{Pb}(\text{Zn}_{1/3}\text{Nb}_{2/3})\text{O}_3$

f) $\text{Pb}(\text{Sc}_{1/2}\text{Ta}_{1/2})\text{O}_3$

as well as combinations of the compounds a) to f) with PbTiO_3 and $\text{Pb}(\text{Mg}_{1/3}\text{Nb}_{2/3})\text{O}_3$ with and without excess lead.

All these ferroelectric ceramic materials have a high, voltage-dependent relative dielectric constant ϵ_r .

In another preferred embodiment, the first electrode and/or the second electrode comprise(s) at least a first and a second electrically conducting layer.

It is preferred that the first electrically conducting layer of the electrodes comprises Ti, Cr, Ni_xCr_y ($0 \leq x \leq 1$, $0 \leq y \leq 1$) or Ti_xW_y ($0 \leq x \leq 1$, $0 \leq y \leq 1$). These layers serve as adhesion layers.

It is furthermore preferred that the second electrically conducting layer of the electrodes comprises a metal or an alloy.

The electric current is mainly passed by the second, well conducting layer. A high conductivity of the materials used leads to a low effective series resistance (ESR) and a low parasitic inductance (ESL).

In a preferred embodiment it is provided that the carrier substrate comprises a ceramic material, a ceramic material with a glass planarization layer, a glass-ceramic material, a glass material, or silicon.

A carrier substrate made of a ceramic material, a ceramic material with a glass planarization layer, a glass-ceramic material, or a glass material can be inexpensively manufactured, so that the process cost for these components can be kept low. If the passive ceramic component is integrated into an IC, the carrier substrate will be of silicon, possibly provided with an SiO_2 passivating layer.

A further preferred embodiment is characterized in that the dielectric comprises multiple layers.

The use of multiple layers, for example double, triple or quadruple layers renders it possible to compensate for the unfavorable temperature behavior of some ferroelectric materials and to improve the temperature dependence of the capacitance value C.

It is also preferred that a protective layer of an inorganic material and/or an organic material is laid over the entire component.

The protective layer protects the subjacent layers against mechanical loads and against corrosion caused by moisture.

The invention also relates to components, in particular tunable filters or delay lines or voltage-controlled oscillators, which comprise as their capacitive component a ceramic passive component which comprises a carrier substrate, at least a first electrode disposed thereon, at least a dielectric disposed thereon, and at least a second electrode disposed thereon, which is characterized in that the dielectric comprises a ferroelectric ceramic material with a voltage-dependent relative dielectric constant ϵ_r .

The use of the component according to the invention, for example, in a tunable RCL filter, a passive delay line with electrically tunable delay time, or as a replacement for a variable-capacitance diode in voltage-controlled oscillators is advantageous because the component according to the invention can be mounted together with other components on a substrate, so that inexpensive circuits of small constructional dimensions can be manufactured.

The invention furthermore relates to the use of a ceramic passive component which comprises a carrier substrate, at least a first electrode disposed thereon, at least a dielectric with a voltage-dependent relative dielectric constant ϵ_r disposed thereon, and at least a second electrode disposed thereon, as a capacitive component.

The invention will be explained in more detail below with reference to five Figures and three embodiments, where

Fig. 1 in a diagrammatic, cross-sectional view shows the construction of a ceramic passive component,

Fig. 2 plots the capacitance as a function of the applied voltage in a ceramic passive component according to the invention,

Fig. 3 is the circuit diagram of an RCL filter,

Fig. 4 shows the filter characteristic of an RCL filter which comprises a component according to the invention as its capacitive component, and

Fig. 5 is the circuit diagram of a passive LC delay member.

In Fig. 1, a ceramic passive component comprises a carrier substrate 1 which is made, for example, from a ceramic material, a ceramic material with a glass planarization layer, a glass-ceramic material, a glass material, or silicon with a passivating layer. On the carrier substrate there is a first electrode 2 which comprises a first electrically conducting layer 3 of, for example, Ti, Cr, Ni_xCr_y ($0 \leq x \leq 1$, $0 \leq y \leq 1$) or Ti_xW_y ($0 \leq x \leq 1$, $0 \leq y \leq 1$) and a second electrically conducting layer 4 comprising, for example, Pt, Ag, Ir, $\text{Ag}_{1-x}\text{Pt}_x$ ($0 \leq x \leq 1$), Ni, Cu, W, $\text{Ag}_{1-x}\text{Pd}_x$ ($0 \leq x \leq 1$), Al, Al doped with Cu, Al doped with Si or Al doped with Mg. A dielectric 5, for example made of $\text{Pb}(\text{Zr}_x\text{Ti}_{1-x})\text{O}_3$ ($0 \leq x \leq 1$) with and without excess lead, $\text{Ba}_{1-x}\text{Sr}_x\text{TiO}_3$ ($0 \leq x \leq 1$), $\text{Pb}_{1-1.5y}\text{La}_y(\text{Zr}_x\text{Ti}_{1-x})\text{O}_3$ ($0 \leq x \leq 1$, $0 \leq y \leq 0.2$), $\text{Pb}(\text{Zr}_x\text{Ti}_{1-x})\text{O}_3$ ($0 \leq x \leq 1$) doped with Nb, $\text{Pb}_{1-\alpha y}\text{La}_y\text{TiO}_3$ ($0 \leq y \leq 0.3$, $1.3 \leq \alpha \leq 1.5$), $(\text{Pb,Ca})\text{TiO}_3$, BaTiO_3 with and without dopants,

$\text{SrZr}_x\text{Ti}_{1-x}\text{O}_3$ ($0 \leq x \leq 1$) with and without Mn dopants, $\text{BaZr}_x\text{Ti}_{1-x}\text{O}_3$ ($0 \leq x \leq 1$), SrTiO_3 doped with, for example, La, Nb, Fe or Mn,

$[\text{Pb}(\text{Mg}_{1/3}\text{Nb}_{2/3})\text{O}_3]_x - [\text{PbTiO}_3]_{1-x}$ ($0 \leq x \leq 1$),

$(\text{Pb}, \text{Ba}, \text{Sr})(\text{Mg}_{1/3}\text{Nb}_{2/3})_x\text{Ti}_y(\text{Zn}_{1/3}\text{Nb}_{2/3})_{1-x-y}\text{O}_3$ ($0 \leq x \leq 1$, $0 \leq y \leq 1$, $x + y \leq 1$),

5 $\text{PbNb}_{4/5x}((\text{Zr}_{0.6}\text{Sn}_{0.4})_{1-y}\text{Ti}_y)_{1-x}\text{O}_3$ ($0 \leq x \leq 0.9$, $0 \leq y \leq 1$), $(\text{Ba}_{1-x}\text{Ca}_x)\text{TiO}_3$ ($0 \leq x \leq 1$),

$(\text{Ba}_{1-x}\text{Sr}_x)\text{TiO}_3$ ($0 \leq x \leq 1$), $(\text{Ba}_{1-x}\text{Pb}_x)\text{TiO}_3$ ($0 \leq x \leq 1$), $(\text{Ba}_{1-x}\text{Sr}_x)(\text{Ti}_{1-x}\text{Zr}_x)\text{O}_3$

($0 \leq x \leq 1$, $0 \leq y \leq 1$),

a) $\text{Pb}(\text{Mg}_{1/2}\text{W}_{1/2})\text{O}_3$

b) $\text{Pb}(\text{Fe}_{1/2}\text{Nb}_{1/2})\text{O}_3$

10 c) $\text{Pb}(\text{Fe}_{2/3}\text{W}_{1/3})\text{O}_3$

d) $\text{Pb}(\text{Ni}_{1/3}\text{Nb}_{2/3})\text{O}_3$

e) $\text{Pb}(\text{Zn}_{1/3}\text{Nb}_{2/3})\text{O}_3$

f) $\text{Pb}(\text{Sc}_{1/2}\text{Ta}_{1/2})\text{O}_3$

as well as combinations of the compounds a) to f) with PbTiO_3 and $\text{Pb}(\text{Mg}_{1/3}\text{Nb}_{2/3})\text{O}_3$ with and

15 without excess lead is provided on the first electrode 2. On the dielectric 5 there is a second electrode 6 which is made of, for example, Pt, Ag, Ir, $\text{Ag}_{1-x}\text{Pt}_x$ ($0 \leq x \leq 1$), Ni, Cu, W, $\text{Ag}_{1-x}\text{Pd}_x$ ($0 \leq x \leq 1$), Al, Al doped with Cu, Al doped with Si or Al doped with Mg or YBa_2CuO_x . A

protective layer 7 of an organic and/or inorganic material is provided over the second

electrode 6. The organic material used may be, for example, polybenzocyclobutene or

20 polyimide, and the inorganic material may be, for example, Si_3N_4 , SiO_2 or $\text{Si}_x\text{O}_y\text{N}_z$ ($0 \leq x \leq 1$, $0 \leq y \leq 1$, $0 \leq z \leq 1$).

Alternatively, the first electrode 2 may comprise only one electrically

conducting layer of, for example, Pt, Ag, Ir, $\text{Ag}_{1-x}\text{Pt}_x$ ($0 \leq x \leq 1$), Ni, Cu, W, $\text{Ag}_{1-x}\text{Pd}_x$ ($0 \leq x \leq 1$), Al, Al doped with Cu, Al doped with Si, or Al doped with Mg, or YBa_2CuO_x . In addition,

25 the second electrode 6 may comprise at least a first and a second electrically conducting layer.

The first electrically conducting layer may then comprise, for example, Ti, Cr, Ni_xCr_y ($0 \leq x \leq 1$, $0 \leq y \leq 1$) or Ti_xW_y ($0 \leq x \leq 1$, $0 \leq y \leq 1$). The material used for the second electrically

conducting layer may be, for example, Pt, Ag, Ir, $\text{Ag}_{1-x}\text{Pt}_x$ ($0 \leq x \leq 1$), Ni, Cu, W, $\text{Ag}_{1-x}\text{Pd}_x$ ($0 \leq x \leq 1$), Al, Al doped with Cu, Al doped with Si or Al doped with Mg.

30 Yet further, for example third, fourth, and fifth electrically conducting layers

may be provided on the respective second electrically conducting layers of the electrodes 2

and 6 as long as suitable combinations of the individual materials are formed. Materials which

are suitable for forming a third electrically conducting layer are, for example, Ti, Ir, Ag, Cr,

Al, IrO_x ($0 \leq x \leq 2$), Ru, $\text{Ru}_x\text{Pt}_{1-x}$ ($0 \leq x \leq 1$), $\text{Pt}_x\text{Al}_{1-x}$ ($0 \leq x \leq 1$), RhO_x ($0 \leq x \leq 2$), $\text{Pt}_x\text{Rh}_{1-x}$ ($0 \leq x \leq 1$), or ITO. A fourth electrically conducting layer may comprise, for example, IrO_x ($0 \leq x \leq 2$), RuO_x ($0 \leq x \leq 2$), $\text{Ru}_x\text{Pt}_{1-x}$ ($0 \leq x \leq 1$), $\text{Pt}_x\text{Al}_{1-x}$ ($0 \leq x \leq 1$), RhO_x ($0 \leq x \leq 2$), $\text{Pt}_x\text{Rh}_{1-x}$ ($0 \leq x \leq 1$), or ITO. A fifth electrically conducting layer may be formed from, for example, RuO_x ($0 \leq x \leq 2$) or $\text{Ru}_x\text{Pt}_{1-x}$ ($0 \leq x \leq 1$).

At least a first and a second current supply contact may be provided at either side of the ceramic passive component. A current supply contact may be, for example, an electroplated SMD end contact of Cr/Cu, Ni/Sn or Cr/Cu, Cu/Ni/Sn or Cr/Ni, Pb/Sn or a bump end contact or a contact surface.

The dielectric 5 may also comprise multiple layers, for example double, triple, or quadruple layers.

Furthermore, an anti-reaction layer made of, for example, TiO_2 , Al_2O_3 , ZrTiO_4 or ZrO_2 may be deposited on the carrier substrate 1. If silicon was used for the carrier substrate 1, the carrier substrate 1 may be provided with an SiO_2 passivating layer.

Fig. 3 shows an RCL filter arrangement consisting of a capacitor C1 with a defined capacitance value, a tunable capacitor C2, two resistors R1 and R2, and three inductances L1 to L3. The RCL filter comprises a first series arrangement of a resistor R1, an inductance L1, and a capacitor C1 connected in parallel to a second series arrangement of a resistor R2, an inductance L2, and a capacitor C2. The inductance L3 is connected in series with this parallel circuit and has one of its terminals connected to ground potential. The parallel circuit is thus connected at one side to the inductance L3, while both the potential V_i and the connection terminals 8 and 9 are applied to the other side.

Fig. 5 shows the circuit arrangement of a passive LC delay member consisting of an inductance L4 and a capacitor C4 which are connected to one another. The junction point between the inductance L4 and the capacitor C4 is connected to a tap 10 and has potential V_i . The other connection is at a tap 11. The other terminal of the capacitor C4 is at ground potential.

Embodiments of the invention will be explained in more detail below, showing examples of how the invention may be carried into practice.

First an anti-reaction layer of TiO_2 and then a first electrically conducting layer 3 of Ti (10 nm) were deposited on a carrier substrate 1 of Al_2O_3 with a glass planarization layer. A second electrically conducting layer 4 of Pt (500 nm) was deposited by sputtering on

this first electrically conducting layer 3, and the two layers were structured by photolithography. Subsequently, a dielectric 5 of $\text{PbZr}_{0.53}\text{Ti}_{0.47}\text{O}_3$ with 5% La dotation was deposited in a sol-gel process, tempered at approximately 600 °C in an oxygen atmosphere, and structured by photolithography. The thickness of the dielectric was 0.75 μm . In the next step, a 500 nm Pt layer was deposited and structured photolithographically into an electrode 6. A protective layer 7 of Si_3N_4 and polyimide was deposited over the entire component. In addition, Cr/Cu, Ni/Sn SMD end contacts were fastened on mutually opposed sides of the component so as to serve as current supply contacts.

Fig. 2 shows the gradient of the capacitance of the ceramic passive component as a function of the applied voltage.

To achieve the same tuning range for the capacitance at lower voltages than those shown in Fig.2, ceramic passive components with a thickness of the dielectric 5 of $d = 0.25 \mu\text{m}$ were manufactured in the manner indicated above. At a surface capacitance of 28 nF/mm^2 , a ceramic passive component with a capacitance of 50 pF on an active surface area of approximately 1800 μm^2 ($42.5 \mu\text{m} * 42.5 \mu\text{m}$) was manufactured, as well as a ceramic passive component with a capacitance of 5 pF on an active surface area of approximately 180 μm^2 ($13.4 \mu\text{m} * 13.4 \mu\text{m}$).

The ceramic passive components thus formed were used in mobile telephones instead of variable-capacitance diodes.

A ceramic passive component was manufactured by the method as explained with reference to Embodiment 1 with a capacitance which was tunable in a range from 17 pF to 56 pF.

This ceramic passive component was used for realizing a tunable RCL filter which is to show a strong damping either at 900 MHz or at 1800 MHz. A capacitor C1 with a defined capacitance value and a tunable capacitor C2 were for this purpose combined with two resistors R1 and R2 and three inductances L1 to L3 into an RCL combination in accordance with the circuit arrangement of Fig. 3. The following were the values:

R1 = 5 Ω , L1 = 0.26 nH, C1 = 2.8 nF, and
R2 = 0.5 Ω , L2 = 0.26 nH, C2 = variable between 17 and 56 pF, and
L3 = 0.3 nH.

The application of a DC voltage of a few volts is capable of varying the capacitance value of the capacitor C2 between 17 and 56 pF, whereby the region having a

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The delay time t_d , which is given by: $t_d = \sqrt{L \cdot C}$, can be shortened from 4 ns at a capacitance value of 2.8 nF to 2.8 ns in that the capacitance is changed to 1.4 nF.

CLAIMS:

1. A ceramic passive component which comprises a carrier substrate (1),
at least a first electrode (2) disposed thereon,
at least a dielectric (5) disposed thereon, and
at least a second electrode (6) disposed thereon,
- 5 characterized in that the dielectric (5) comprises a ferroelectric ceramic material with a
voltage-dependent relative dielectric constant ϵ_r .
2. A ceramic passive component as claimed in claim 1, characterized in that the
following is chosen as the ferroelectric ceramic material with a voltage-dependent dielectric
10 constant ϵ_r :
 $\text{Pb}(\text{Zr}_x\text{Ti}_{1-x})\text{O}_3$ ($0 \leq x \leq 1$) with and without excess lead, $\text{Ba}_{1-x}\text{Sr}_x\text{TiO}_3$ ($0 \leq x \leq 1$),
 $\text{Pb}_{1-1.5y}\text{La}_y(\text{Zr}_x\text{Ti}_{1-x})\text{O}_3$ ($0 \leq x \leq 1$, $0 \leq y \leq 0.2$), $\text{Pb}(\text{Zr}_x\text{Ti}_{1-x})\text{O}_3$ ($0 \leq x \leq 1$) doped with Nb, $\text{Pb}_{1-\alpha y}\text{La}_y\text{TiO}_3$ ($0 \leq y \leq 0.3$, $1.3 \leq \alpha \leq 1.5$), $(\text{Pb}, \text{Ca})\text{TiO}_3$, BaTiO_3 with and without dopants,
 $\text{SrZr}_x\text{Ti}_{1-x}\text{O}_3$ ($0 \leq x \leq 1$) with and without Mn dopants, $\text{BaZr}_x\text{Ti}_{1-x}\text{O}_3$ ($0 \leq x \leq 1$), SrTiO_3 doped
15 with, for example, La, Nb, Fe or Mn,
 $[\text{Pb}(\text{Mg}_{1/3}\text{Nb}_{2/3})\text{O}_3]_x - [\text{PbTiO}_3]_{1-x}$ ($0 \leq x \leq 1$),
 $(\text{Pb}, \text{Ba}, \text{Sr})(\text{Mg}_{1/3}\text{Nb}_{2/3})_x\text{Ti}_y(\text{Zn}_{1/3}\text{Nb}_{2/3})_{1-x-y}\text{O}_3$ ($0 \leq x \leq 1$, $0 \leq y \leq 1$, $x + y \leq 1$),
 $\text{PbNb}_{4/5x}((\text{Zr}_{0.6}\text{Sn}_{0.4})_{1-y}\text{Ti}_y)_{1-x}\text{O}_3$ ($0 \leq x \leq 0.9$, $0 \leq y \leq 1$), $(\text{Ba}_{1-x}\text{Ca}_x)\text{TiO}_3$ ($0 \leq x \leq 1$),
 $(\text{Ba}_{1-x}\text{Sr}_x)\text{TiO}_3$ ($0 \leq x \leq 1$), $(\text{Ba}_{1-x}\text{Pb}_x)\text{TiO}_3$ ($0 \leq x \leq 1$), $(\text{Ba}_{1-x}\text{Sr}_x)(\text{Ti}_{1-x}\text{Zr}_x)\text{O}_3$
20 ($0 \leq x \leq 1$, $0 \leq y \leq 1$),
a) $\text{Pb}(\text{Mg}_{1/2}\text{W}_{1/2})\text{O}_3$
b) $\text{Pb}(\text{Fe}_{1/2}\text{Nb}_{1/2})\text{O}_3$
c) $\text{Pb}(\text{Fe}_{2/3}\text{W}_{1/3})\text{O}_3$
d) $\text{Pb}(\text{Ni}_{1/3}\text{Nb}_{2/3})\text{O}_3$
25 e) $\text{Pb}(\text{Zn}_{1/3}\text{Nb}_{2/3})\text{O}_3$
f) $\text{Pb}(\text{Sc}_{1/2}\text{Ta}_{1/2})\text{O}_3$
as well as combinations of the compounds a) to f) with PbTiO_3 and $\text{Pb}(\text{Mg}_{1/3}\text{Nb}_{2/3})\text{O}_3$ with and
without excess lead.

3. A ceramic passive component as claimed in claim 1, characterized in that the first electrode (2) and/or the second electrode (6) comprise(s) at least a first and a second electrically conducting layer.

5 4. A ceramic passive component as claimed in claim 3, characterized in that the first electrically conducting layer of the electrodes (2, 6) comprises Ti, Cr, Ni_xCr_y ($0 \leq x \leq 1$, $0 \leq y \leq 1$) or Ti_xW_y ($0 \leq x \leq 1$, $0 \leq y \leq 1$).

10 5. A ceramic passive component as claimed in claim 3, characterized in that the second electrically conducting layer of the electrodes (2, 6) comprises a metal or an alloy.

15 6. A ceramic passive component as claimed in claim 1, characterized in that the carrier substrate (1) comprises a ceramic material, a ceramic material with a glass planarization layer, a glass-ceramic material, a glass material, or silicon.

7. A ceramic passive component as claimed in claim 1, characterized in that the dielectric (5) comprises multiple layers.

20 8. A ceramic passive component as claimed in claim 1, characterized in that a protective layer (7) of an inorganic material and/or an organic material is laid over the entire component.

25 9. A voltage-controlled oscillator with as its capacitive component a ceramic passive component which comprises a carrier substrate (1), at least a first electrode (2) disposed thereon, at least a dielectric (5) disposed thereon, and at least a second electrode (6) disposed thereon, characterized in that the dielectric (5) comprises a ferroelectric ceramic material with a voltage-dependent relative dielectric constant ϵ_r .

30 10. A filter with as its capacitive component a ceramic passive component which comprises a carrier substrate (1), at least a first electrode (2) disposed thereon, at least a dielectric (5) disposed thereon, and at least a second electrode (6) disposed thereon, characterized in that the dielectric (5) comprises a ferroelectric ceramic material with a voltage-dependent relative dielectric constant ϵ_r .

11. A delay line with as its capacitive component a ceramic passive component which comprises a carrier substrate (1), at least a first electrode (2) disposed thereon, at least a dielectric (5) disposed thereon, and at least a second electrode (6) disposed thereon, characterized in that the dielectric (5) comprises a ferroelectric ceramic material with a voltage-dependent relative dielectric constant ϵ_r .
12. The use of a ceramic passive component which comprises a carrier substrate (1), at least a first electrode (2) disposed thereon, at least a dielectric (5) with a voltage-dependent relative dielectric constant ϵ_r disposed thereon, and at least a second electrode (6) disposed thereon as a capacitive component.

ABSTRACT:

The invention relates to a passive ceramic component with a carrier substrate (1), a first and a second electrode (2, 6), and a ferroelectric dielectric (5). The electrodes (2, 6) and the dielectric (5) preferably comprise a multilayer structure with at least a first and a second layer. The capacitance value C of the capacitor can be varied through the application of a voltage to the electrodes (2, 6), owing to the field dependence of the dielectric constant ϵ_r of the dielectric (5).

Such components may be used in filter devices or in delay lines or as replacements for variable-capacitance diodes in the manufacture of voltage-controlled oscillators.

Fig. 1

Voltage-dependent thin-film capacitor.

The invention relates to a ceramic passive component which comprises a carrier substrate, at least a first electrode disposed thereon, at least a dielectric disposed thereon, and at least a second electrode disposed thereon. The invention also relates to components in which at least one ceramic passive component with the above construction is used.

5 Variable-capacitance diodes (also called varicaps) are diodes in which the voltage dependence of a pn junction is utilized in practice. Each pn junction forms a capacitor with the p- and the n-zone as the plates and the interposed depletion or blocking layer as the dielectric. The thickness of the depletion layer increases with the applied reverse voltage, so that the capacitance value of the pn junction decreases.

10 Variable-capacitance diodes are available in various embodiments. Typical operating voltages are 12 to 30 V accompanied by a capacitance which is variable by a factor 10 to 20. Lower voltages in a range from 3 to 5 V are usual in mobile telephone applications with a tuning range having a factor between 2 and 4. The capacitance values of the diodes usually vary between 20 and 40 pF in this case. These semiconductor components are used
15 inter alia in the manufacture of voltage-controlled oscillators (VCOs).

The present trend is towards lower voltages and high frequencies (GHz) especially in the field of mobile telephony. The construction of variable-capacitance diodes for this application, however, becomes increasingly difficult, especially if the dimensions of the components have to be as small as possible. The semiconductor components also come close
20 to the limits of their possibilities in view of their effective series resistance. In addition, the cost of manufacture of variable-capacitance diodes is very high.

The invention has for its object to provide a component which has a tunable capacitance as well as a low effective series resistance and which can be inexpensively manufactured.

25 This object is achieved by means of a ceramic passive component which comprises a carrier substrate, at least a first electrode disposed thereon, at least a dielectric disposed thereon, and at least a second electrode disposed thereon, wherein the dielectric comprises a ferroelectric ceramic material with a voltage-dependent relative dielectric constant ϵ_r .

Given certain geometric dimensions (surface area A , electrode spacing d), the capacitance of a capacitor can be calculated from the equation:

$$C = (\epsilon_r \cdot \epsilon_0 \cdot A) / d.$$

A voltage dependence of the capacitance C is thus defined by the voltage dependence of the dielectric constant ϵ_r . Many dielectric materials exhibit a low dielectric constant ϵ_r and a low field dependence $\epsilon_r(E)$. An exception is formed by ferroelectric materials, in which ϵ_r can be changed through the application of an electric field E . The capacitance value C of a capacitor can thus be changed through the application of a voltage to the electrodes.

The advantages of these components are that on the one hand they are not polar, in contrast to variable-capacitance diodes, and on the other hand that they can be manufactured more cheaply than the semiconductor components.

It is to be highly preferred that the following is chosen as the ferroelectric ceramic material with a voltage-dependent dielectric constant ϵ_r :

- $\text{Pb}(\text{Zr}_x\text{Ti}_{1-x})\text{O}_3$ ($0 \leq x \leq 1$) with and without excess lead, $\text{Ba}_{1-x}\text{Sr}_x\text{TiO}_3$ ($0 \leq x \leq 1$),
- $\text{Pb}_{1-1.5y}\text{La}_y(\text{Zr}_x\text{Ti}_{1-x})\text{O}_3$ ($0 \leq x \leq 1$, $0 \leq y \leq 0.2$), $\text{Pb}(\text{Zr}_x\text{Ti}_{1-x})\text{O}_3$ ($0 \leq x \leq 1$) doped with Nb, $\text{Pb}_{1-\alpha y}\text{La}_y\text{TiO}_3$ ($0 \leq y \leq 0.3$, $1.3 \leq \alpha \leq 1.5$), $(\text{Pb,Ca})\text{TiO}_3$, BaTiO_3 with and without dopants, $\text{SrZr}_x\text{Ti}_{1-x}\text{O}_3$ ($0 \leq x \leq 1$) with and without Mn dopants, $\text{BaZr}_x\text{Ti}_{1-x}\text{O}_3$ ($0 \leq x \leq 1$), SrTiO_3 doped with, for example, La, Nb, Fe or Mn,
- $[\text{Pb}(\text{Mg}_{1/3}\text{Nb}_{2/3})\text{O}_3]_x - [\text{PbTiO}_3]_{1-x}$ ($0 \leq x \leq 1$),
- $(\text{Pb,Ba,Sr})(\text{Mg}_{1/3}\text{Nb}_{2/3})_x\text{Ti}_y(\text{Zn}_{1/3}\text{Nb}_{2/3})_{1-x-y}\text{O}_3$ ($0 \leq x \leq 1$, $0 \leq y \leq 1$, $x + y \leq 1$),
- $\text{PbNb}_{4/5x}((\text{Zr}_{0.6}\text{Sn}_{0.4})_{1-y}\text{Ti}_y)_{1-x}\text{O}_3$ ($0 \leq x \leq 0.9$, $0 \leq y \leq 1$), $(\text{Ba}_{1-x}\text{Ca}_x)\text{TiO}_3$ ($0 \leq x \leq 1$), $(\text{Ba}_{1-x}\text{Sr}_x)\text{TiO}_3$ ($0 \leq x \leq 1$), $(\text{Ba}_{1-x}\text{Pb}_x)\text{TiO}_3$ ($0 \leq x \leq 1$), $(\text{Ba}_{1-x}\text{Sr}_x)(\text{Ti}_{1-x}\text{Zr}_x)\text{O}_3$ ($0 \leq x \leq 1$, $0 \leq y \leq 1$),
- a) $\text{Pb}(\text{Mg}_{1/2}\text{W}_{1/2})\text{O}_3$
- b) $\text{Pb}(\text{Fe}_{1/2}\text{Nb}_{1/2})\text{O}_3$
- c) $\text{Pb}(\text{Fe}_{2/3}\text{W}_{1/3})\text{O}_3$
- d) $\text{Pb}(\text{Ni}_{1/3}\text{Nb}_{2/3})\text{O}_3$
- e) $\text{Pb}(\text{Zn}_{1/3}\text{Nb}_{2/3})\text{O}_3$
- f) $\text{Pb}(\text{Sc}_{1/2}\text{Ta}_{1/2})\text{O}_3$
- as well as combinations of the compounds a) to f) with PbTiO_3 and $\text{Pb}(\text{Mg}_{1/3}\text{Nb}_{2/3})\text{O}_3$ with and without excess lead.

All these ferroelectric ceramic materials have a high, voltage-dependent relative dielectric constant ϵ_r .

In another preferred embodiment, the first electrode and/or the second electrode comprise(s) at least a first and a second electrically conducting layer.

It is preferred that the first electrically conducting layer of the electrodes comprises Ti, Cr, Ni_xCr_y ($0 \leq x \leq 1$, $0 \leq y \leq 1$) or Ti_xW_y ($0 \leq x \leq 1$, $0 \leq y \leq 1$). These layers serve as adhesion layers.

It is furthermore preferred that the second electrically conducting layer of the electrodes comprises a metal or an alloy.

The electric current is mainly passed by the second, well conducting layer. A high conductivity of the materials used leads to a low effective series resistance (ESR) and a low parasitic inductance (ESL).

In a preferred embodiment it is provided that the carrier substrate comprises a ceramic material, a ceramic material with a glass planarization layer, a glass-ceramic material, a glass material, or silicon.

A carrier substrate made of a ceramic material, a ceramic material with a glass planarization layer, a glass-ceramic material, or a glass material can be inexpensively manufactured, so that the process cost for these components can be kept low. If the passive ceramic component is integrated into an IC, the carrier substrate will be of silicon, possibly provided with an SiO_2 passivating layer.

A further preferred embodiment is characterized in that the dielectric comprises multiple layers.

The use of multiple layers, for example double, triple or quadruple layers renders it possible to compensate for the unfavorable temperature behavior of some ferroelectric materials and to improve the temperature dependence of the capacitance value C.

It is also preferred that a protective layer of an inorganic material and/or an organic material is laid over the entire component.

The protective layer protects the subjacent layers against mechanical loads and against corrosion caused by moisture.

The invention also relates to components, in particular tunable filters or delay lines or voltage-controlled oscillators, which comprise as their capacitive component a ceramic passive component which comprises a carrier substrate, at least a first electrode disposed thereon, at least a dielectric disposed thereon, and at least a second electrode disposed thereon, which is characterized in that the dielectric comprises a ferroelectric ceramic material with a voltage-dependent relative dielectric constant ϵ_r .

The use of the component according to the invention, for example, in a tunable RCL filter, a passive delay line with electrically tunable delay time, or as a replacement for a variable-capacitance diode in voltage-controlled oscillators is advantageous because the component according to the invention can be mounted together with other components on a substrate, so that inexpensive circuits of small constructional dimensions can be manufactured.

The invention furthermore relates to the use of a ceramic passive component which comprises a carrier substrate, at least a first electrode disposed thereon, at least a dielectric with a voltage-dependent relative dielectric constant ϵ_r disposed thereon, and at least a second electrode disposed thereon, as a capacitive component.

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The invention will be explained in more detail below with reference to five Figures and three embodiments, where

Fig. 1 in a diagrammatic, cross-sectional view shows the construction of a ceramic passive component,

Fig. 2 plots the capacitance as a function of the applied voltage in a ceramic passive component according to the invention,

Fig. 3 is the circuit diagram of an RCL filter,

Fig. 4 shows the filter characteristic of an RCL filter which comprises a component according to the invention as its capacitive component, and

Fig. 5 is the circuit diagram of a passive LC delay member.

In Fig. 1, a ceramic passive component comprises a carrier substrate 1 which is made, for example, from a ceramic material, a ceramic material with a glass planarization layer, a glass-ceramic material, a glass material, or silicon with a passivating layer. On the carrier substrate there is a first electrode 2 which comprises a first electrically conducting layer 3 of, for example, Ti, Cr, Ni_xCr_y ($0 \leq x \leq 1$, $0 \leq y \leq 1$) or Ti_xW_y ($0 \leq x \leq 1$, $0 \leq y \leq 1$) and a second electrically conducting layer 4 comprising, for example, Pt, Ag, Ir, $\text{Ag}_{1-x}\text{Pt}_x$ ($0 \leq x \leq 1$), Ni, Cu, W, $\text{Ag}_{1-x}\text{Pd}_x$ ($0 \leq x \leq 1$), Al, Al doped with Cu, Al doped with Si or Al doped with Mg. A dielectric 5, for example made of $\text{Pb}(\text{Zr}_x\text{Ti}_{1-x})\text{O}_3$ ($0 \leq x \leq 1$) with and without excess lead, $\text{Ba}_{1-x}\text{Sr}_x\text{TiO}_3$ ($0 \leq x \leq 1$), $\text{Pb}_{1-1.5y}\text{La}_y(\text{Zr}_x\text{Ti}_{1-x})\text{O}_3$ ($0 \leq x \leq 1$, $0 \leq y \leq 0.2$), $\text{Pb}(\text{Zr}_x\text{Ti}_{1-x})\text{O}_3$ ($0 \leq x \leq 1$) doped with Nb, $\text{Pb}_{1-\alpha}\text{La}_\alpha\text{TiO}_3$ ($0 \leq y \leq 0.3$, $1.3 \leq \alpha \leq 1.5$), $(\text{Pb,Ca})\text{TiO}_3$, BaTiO_3 with and without dopants,

SrZr_xTi_{1-x}O₃ ($0 \leq x \leq 1$) with and without Mn dopants, BaZr_xTi_{1-x}O₃ ($0 \leq x \leq 1$), SrTiO₃ doped with, for example, La, Nb, Fe or Mn,

[Pb(Mg_{1/3}Nb_{2/3})O₃]_x-[PbTiO₃]_{1-x} ($0 \leq x \leq 1$),

(Pb,Ba,Sr)(Mg_{1/3}Nb_{2/3})_xTi_y(Zn_{1/3}Nb_{2/3})_{1-x-y}O₃ ($0 \leq x \leq 1$, $0 \leq y \leq 1$, $x + y \leq 1$),

5 PbNb_{4/5x}((Zr_{0.6}Sn_{0.4})_{1-y}Ti_y)_{1-x}O₃ ($0 \leq x \leq 0.9$, $0 \leq y \leq 1$), (Ba_{1-x}Ca_x)TiO₃ ($0 \leq x \leq 1$),

(Ba_{1-x}Sr_x)TiO₃ ($0 \leq x \leq 1$), (Ba_{1-x}Pb_x)TiO₃ ($0 \leq x \leq 1$), (Ba_{1-x}Sr_x)(Ti_{1-x}Zr_x)O₃

($0 \leq x \leq 1$, $0 \leq y \leq 1$),

a) Pb(Mg_{1/2}W_{1/2})O₃

b) Pb(Fe_{1/2}Nb_{1/2})O₃

10 c) Pb(Fe_{2/3}W_{1/3})O₃

d) Pb(Ni_{1/3}Nb_{2/3})O₃

e) Pb(Zn_{1/3}Nb_{2/3})O₃

f) Pb(Sc_{1/2}Ta_{1/2})O₃

as well as combinations of the compounds a) to f) with PbTiO₃ and Pb(Mg_{1/3}Nb_{2/3})O₃ with and

15 without excess lead is provided on the first electrode 2. On the dielectric 5 there is a second electrode 6 which is made of, for example, Pt, Ag, Ir, Ag_{1-x}Pt_x ($0 \leq x \leq 1$), Ni, Cu, W, Ag_{1-x}Pd_x ($0 \leq x \leq 1$), Al, Al doped with Cu, Al doped with Si or Al doped with Mg or YBa₂CuO_x. A

protective layer 7 of an organic and/or inorganic material is provided over the second

electrode 6. The organic material used may be, for example, polybenzocyclobutene or

20 polyimide, and the inorganic material may be, for example, Si₃N₄, SiO₂ or Si_xO_yN_z ($0 \leq x \leq 1$, $0 \leq y \leq 1$, $0 \leq z \leq 1$).

Alternatively, the first electrode 2 may comprise only one electrically

conducting layer of, for example, Pt, Ag, Ir, Ag_{1-x}Pt_x ($0 \leq x \leq 1$), Ni, Cu, W, Ag_{1-x}Pd_x ($0 \leq x \leq 1$), Al, Al doped with Cu, Al doped with Si, or Al doped with Mg, or YBa₂CuO_x. In addition,

25 the second electrode 6 may comprise at least a first and a second electrically conducting layer.

The first electrically conducting layer may then comprise, for example, Ti, Cr, Ni_xCr_y ($0 \leq x \leq 1$, $0 \leq y \leq 1$) or Ti_xW_y ($0 \leq x \leq 1$, $0 \leq y \leq 1$). The material used for the second electrically

conducting layer may be, for example, Pt, Ag, Ir, Ag_{1-x}Pt_x ($0 \leq x \leq 1$), Ni, Cu, W, Ag_{1-x}Pd_x ($0 \leq x \leq 1$), Al, Al doped with Cu, Al doped with Si or Al doped with Mg.

30 Yet further, for example third, fourth, and fifth electrically conducting layers may be provided on the respective second electrically conducting layers of the electrodes 2 and 6 as long as suitable combinations of the individual materials are formed. Materials which are suitable for forming a third electrically conducting layer are, for example, Ti, Ir, Ag, Cr,

Al, IrO_x ($0 \leq x \leq 2$), Ru, $\text{Ru}_x\text{Pt}_{1-x}$ ($0 \leq x \leq 1$), $\text{Pt}_x\text{Al}_{1-x}$ ($0 \leq x \leq 1$), RhO_x ($0 \leq x \leq 2$), $\text{Pt}_x\text{Rh}_{1-x}$ ($0 \leq x \leq 1$), or ITO. A fourth electrically conducting layer may comprise, for example, IrO_x ($0 \leq x \leq 2$), RuO_x ($0 \leq x \leq 2$), $\text{Ru}_x\text{Pt}_{1-x}$ ($0 \leq x \leq 1$), $\text{Pt}_x\text{Al}_{1-x}$ ($0 \leq x \leq 1$), RhO_x ($0 \leq x \leq 2$), $\text{Pt}_x\text{Rh}_{1-x}$ ($0 \leq x \leq 1$), or ITO. A fifth electrically conducting layer may be formed from, for example, RuO_x ($0 \leq x \leq 2$) or $\text{Ru}_x\text{Pt}_{1-x}$ ($0 \leq x \leq 1$).

At least a first and a second current supply contact may be provided at either side of the ceramic passive component. A current supply contact may be, for example, an electroplated SMD end contact of Cr/Cu, Ni/Sn or Cr/Cu, Cu/Ni/Sn or Cr/Ni, Pb/Sn or a bump end contact or a contact surface.

The dielectric 5 may also comprise multiple layers, for example double, triple, or quadruple layers.

Furthermore, an anti-reaction layer made of, for example, TiO_2 , Al_2O_3 , ZrTiO_4 or ZrO_2 may be deposited on the carrier substrate 1. If silicon was used for the carrier substrate 1, the carrier substrate 1 may be provided with an SiO_2 passivating layer.

Fig. 3 shows an RCL filter arrangement consisting of a capacitor C1 with a defined capacitance value, a tunable capacitor C2, two resistors R1 and R2, and three inductances L1 to L3. The RCL filter comprises a first series arrangement of a resistor R1, an inductance L1, and a capacitor C1 connected in parallel to a second series arrangement of a resistor R2, an inductance L2, and a capacitor C2. The inductance L3 is connected in series with this parallel circuit and has one of its terminals connected to ground potential. The parallel circuit is thus connected at one side to the inductance L3, while both the potential V_t and the connection terminals 8 and 9 are applied to the other side.

Fig. 5 shows the circuit arrangement of a passive LC delay member consisting of an inductance L4 and a capacitor C4 which are connected to one another. The junction point between the inductance L4 and the capacitor C4 is connected to a tap 10 and has potential V_t . The other connection is at a tap 11. The other terminal of the capacitor C4 is at ground potential.

Embodiments of the invention will be explained in more detail below, showing examples of how the invention may be carried into practice.

First an anti-reaction layer of TiO_2 and then a first electrically conducting layer 3 of Ti (10 nm) were deposited on a carrier substrate 1 of Al_2O_3 with a glass planarization layer. A second electrically conducting layer 4 of Pt (500 nm) was deposited by sputtering on

this first electrically conducting layer 3, and the two layers were structured by photolithography. Subsequently, a dielectric 5 of $\text{PbZr}_{0.53}\text{Ti}_{0.47}\text{O}_3$ with 5% La dotation was deposited in a sol-gel process, tempered at approximately 600 °C in an oxygen atmosphere, and structured by photolithography. The thickness of the dielectric was 0.75 μm . In the next step, a 500 nm Pt layer was deposited and structured photolithographically into an electrode 6. A protective layer 7 of Si_3N_4 and polyimide was deposited over the entire component. In addition, Cr/Cu, Ni/Sn SMD end contacts were fastened on mutually opposed sides of the component so as to serve as current supply contacts.

Fig. 2 shows the gradient of the capacitance of the ceramic passive component as a function of the applied voltage.

To achieve the same tuning range for the capacitance at lower voltages than those shown in Fig.2, ceramic passive components with a thickness of the dielectric 5 of $d = 0.25 \mu\text{m}$ were manufactured in the manner indicated above. At a surface capacitance of 28 nF/mm^2 , a ceramic passive component with a capacitance of 50 pF on an active surface area of approximately 1800 μm^2 ($42.5 \mu\text{m} * 42.5 \mu\text{m}$) was manufactured, as well as a ceramic passive component with a capacitance of 5 pF on an active surface area of approximately 180 μm^2 ($13.4 \mu\text{m} * 13.4 \mu\text{m}$).

The ceramic passive components thus formed were used in mobile telephones instead of variable-capacitance diodes.

A ceramic passive component was manufactured by the method as explained with reference to Embodiment 1 with a capacitance which was tunable in a range from 17 pF to 56 pF.

This ceramic passive component was used for realizing a tunable RCL filter which is to show a strong damping either at 900 MHz or at 1800 MHz. A capacitor C1 with a defined capacitance value and a tunable capacitor C2 were for this purpose combined with two resistors R1 and R2 and three inductances L1 to L3 into an RCL combination in accordance with the circuit arrangement of Fig. 3. The following were the values:

R1 = 5 Ω , L1 = 0.26 nH, C1 = 2.8 nF, and

R2 = 0.5 Ω , L2 = 0.26 nH, C2 = variable between 17 and 56 pF, and

L3 = 0.3 nH.

The application of a DC voltage of a few volts is capable of varying the capacitance value of the capacitor C2 between 17 and 56 pF, whereby the region having a

strong absorption in the filter characteristic can be shifted back and forth between 900 and 1800 MHz, as is shown in Fig. 4. Curve I in this Fig. corresponds to a capacitance value of the capacitor C2 of 56 pF and curve II to a capacitance value of 17 pF.

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A ceramic passive component was manufactured by the method as explained with reference to Embodiment 1 with a capacitance which was tunable in a range from 1.4 nF to 2.8 nF through the application of a DC voltage of a few volts.

The ceramic passive component was used for realizing a passive LC delay member with an electrically changeable delay time t_d . The tunable capacitor C4 was for this purpose combined with an inductance L4 of 5.7 nH, as shown in Fig. 5.

The delay time t_d , which is given by: $t_d = \sqrt{L * C}$, can be shortened from 4 ns at a capacitance value of 2.8 nF to 2.8 ns in that the capacitance is changed to 1.4 nF.

CLAIMS:

1. A ceramic passive component which comprises a carrier substrate (1),
at least a first electrode (2) disposed thereon,
at least a dielectric (5) disposed thereon, and
at least a second electrode (6) disposed thereon,
- 5 characterized in that the dielectric (5) comprises a ferroelectric ceramic material with a
voltage-dependent relative dielectric constant ϵ_r .
2. A ceramic passive component as claimed in claim 1, characterized in that the
following is chosen as the ferroelectric ceramic material with a voltage-dependent dielectric
10 constant ϵ_r :
 $\text{Pb}(\text{Zr}_x\text{Ti}_{1-x})\text{O}_3$ ($0 \leq x \leq 1$) with and without excess lead, $\text{Ba}_{1-x}\text{Sr}_x\text{TiO}_3$ ($0 \leq x \leq 1$),
 $\text{Pb}_{1-1.5y}\text{La}_y(\text{Zr}_x\text{Ti}_{1-x})\text{O}_3$ ($0 \leq x \leq 1$, $0 \leq y \leq 0.2$), $\text{Pb}(\text{Zr}_x\text{Ti}_{1-x})\text{O}_3$ ($0 \leq x \leq 1$) doped with Nb, $\text{Pb}_{1-\alpha y}\text{La}_y\text{TiO}_3$ ($0 \leq y \leq 0.3$, $1.3 \leq \alpha \leq 1.5$), $(\text{Pb}, \text{Ca})\text{TiO}_3$, BaTiO_3 with and without dopants,
 $\text{SrZr}_x\text{Ti}_{1-x}\text{O}_3$ ($0 \leq x \leq 1$) with and without Mn dopants, $\text{BaZr}_x\text{Ti}_{1-x}\text{O}_3$ ($0 \leq x \leq 1$), SrTiO_3 doped
15 with, for example, La, Nb, Fe or Mn,
 $[\text{Pb}(\text{Mg}_{1/3}\text{Nb}_{2/3})\text{O}_3]_x[\text{PbTiO}_3]_{1-x}$ ($0 \leq x \leq 1$),
 $(\text{Pb}, \text{Ba}, \text{Sr})(\text{Mg}_{1/3}\text{Nb}_{2/3})_x\text{Ti}_y(\text{Zn}_{1/3}\text{Nb}_{2/3})_{1-x-y}\text{O}_3$ ($0 \leq x \leq 1$, $0 \leq y \leq 1$, $x + y \leq 1$),
 $\text{PbNb}_{4/5x}((\text{Zr}_{0.6}\text{Sn}_{0.4})_{1-y}\text{Ti}_y)_{1-x}\text{O}_3$ ($0 \leq x \leq 0.9$, $0 \leq y \leq 1$), $(\text{Ba}_{1-x}\text{Ca}_x)\text{TiO}_3$ ($0 \leq x \leq 1$),
 $(\text{Ba}_{1-x}\text{Sr}_x)\text{TiO}_3$ ($0 \leq x \leq 1$), $(\text{Ba}_{1-x}\text{Pb}_x)\text{TiO}_3$ ($0 \leq x \leq 1$), $(\text{Ba}_{1-x}\text{Sr}_x)(\text{Ti}_{1-x}\text{Zr}_x)\text{O}_3$
20 ($0 \leq x \leq 1$, $0 \leq y \leq 1$),
a) $\text{Pb}(\text{Mg}_{1/2}\text{W}_{1/2})\text{O}_3$
b) $\text{Pb}(\text{Fe}_{1/2}\text{Nb}_{1/2})\text{O}_3$
c) $\text{Pb}(\text{Fe}_{2/3}\text{W}_{1/3})\text{O}_3$
d) $\text{Pb}(\text{Ni}_{1/3}\text{Nb}_{2/3})\text{O}_3$
25 e) $\text{Pb}(\text{Zn}_{1/3}\text{Nb}_{2/3})\text{O}_3$
f) $\text{Pb}(\text{Sc}_{1/2}\text{Ta}_{1/2})\text{O}_3$
as well as combinations of the compounds a) to f) with PbTiO_3 and $\text{Pb}(\text{Mg}_{1/3}\text{Nb}_{2/3})\text{O}_3$ with and
without excess lead.

3. A ceramic passive component as claimed in claim 1, characterized in that the first electrode (2) and/or the second electrode (6) comprise(s) at least a first and a second electrically conducting layer.

5 4. A ceramic passive component as claimed in claim 3, characterized in that the first electrically conducting layer of the electrodes (2, 6) comprises Ti, Cr, Ni_xCr_y ($0 \leq x \leq 1$, $0 \leq y \leq 1$) or Ti_xW_y ($0 \leq x \leq 1$, $0 \leq y \leq 1$).

10 5. A ceramic passive component as claimed in claim 3, characterized in that the second electrically conducting layer of the electrodes (2, 6) comprises a metal or an alloy.

15 6. A ceramic passive component as claimed in claim 1, characterized in that the carrier substrate (1) comprises a ceramic material, a ceramic material with a glass planarization layer, a glass-ceramic material, a glass material, or silicon.

7. A ceramic passive component as claimed in claim 1, characterized in that the dielectric (5) comprises multiple layers.

20 8. A ceramic passive component as claimed in claim 1, characterized in that a protective layer (7) of an inorganic material and/or an organic material is laid over the entire component.

25 9. A voltage-controlled oscillator with as its capacitive component a ceramic passive component which comprises a carrier substrate (1), at least a first electrode (2) disposed thereon, at least a dielectric (5) disposed thereon, and at least a second electrode (6) disposed thereon, characterized in that the dielectric (5) comprises a ferroelectric ceramic material with a voltage-dependent relative dielectric constant ϵ_r .

30 10. A filter with as its capacitive component a ceramic passive component which comprises a carrier substrate (1), at least a first electrode (2) disposed thereon, at least a dielectric (5) disposed thereon, and at least a second electrode (6) disposed thereon, characterized in that the dielectric (5) comprises a ferroelectric ceramic material with a voltage-dependent relative dielectric constant ϵ_r .

11. A delay line with as its capacitive component a ceramic passive component which comprises a carrier substrate (1), at least a first electrode (2) disposed thereon, at least a dielectric (5) disposed thereon, and at least a second electrode (6) disposed thereon, characterized in that the dielectric (5) comprises a ferroelectric ceramic material with a voltage-dependent relative dielectric constant ϵ_r .
12. The use of a ceramic passive component which comprises a carrier substrate (1), at least a first electrode (2) disposed thereon, at least a dielectric (5) with a voltage-dependent relative dielectric constant ϵ_r disposed thereon, and at least a second electrode (6) disposed thereon as a capacitive component.

ABSTRACT:

The invention relates to a passive ceramic component with a carrier substrate (1), a first and a second electrode (2, 6), and a ferroelectric dielectric (5). The electrodes (2, 6) and the dielectric (5) preferably comprise a multilayer structure with at least a first and a second layer. The capacitance value C of the capacitor can be varied through the application of a voltage to the electrodes (2, 6), owing to the field dependence of the dielectric constant ϵ_r of the dielectric (5).

Such components may be used in filter devices or in delay lines or as replacements for variable-capacitance diodes in the manufacture of voltage-controlled oscillators.

Fig. 1

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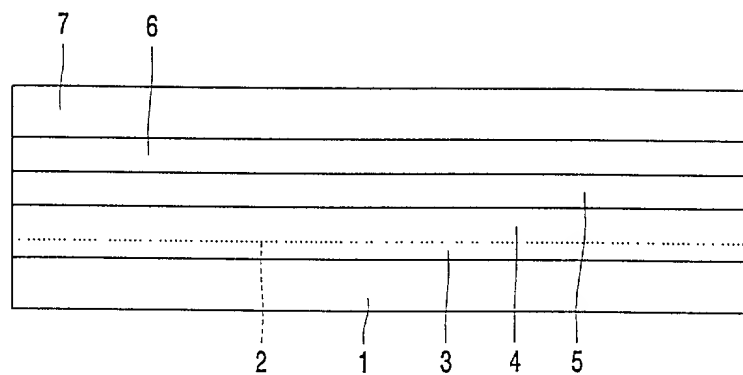


FIG. 1

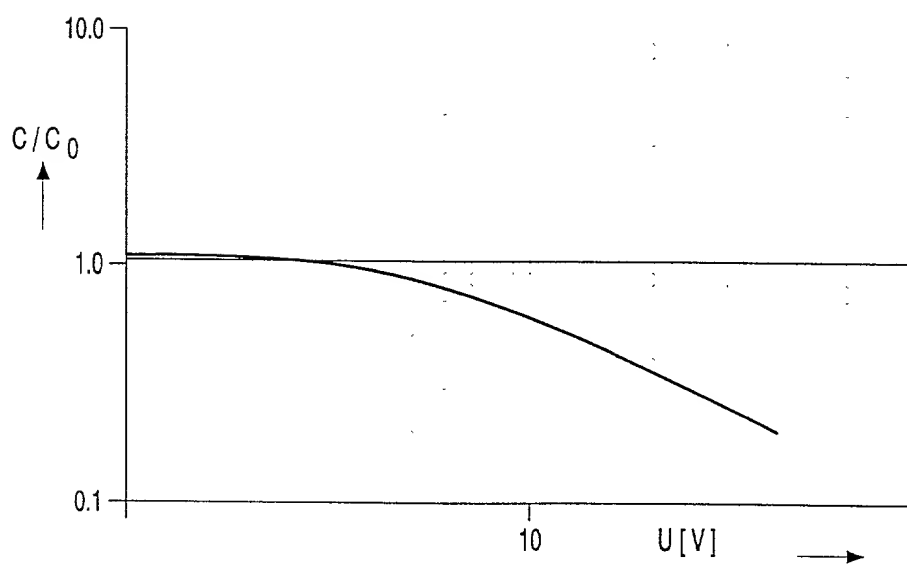


FIG. 2

2/2

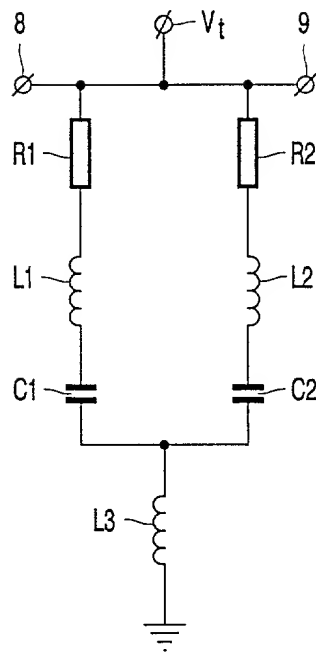


FIG. 3

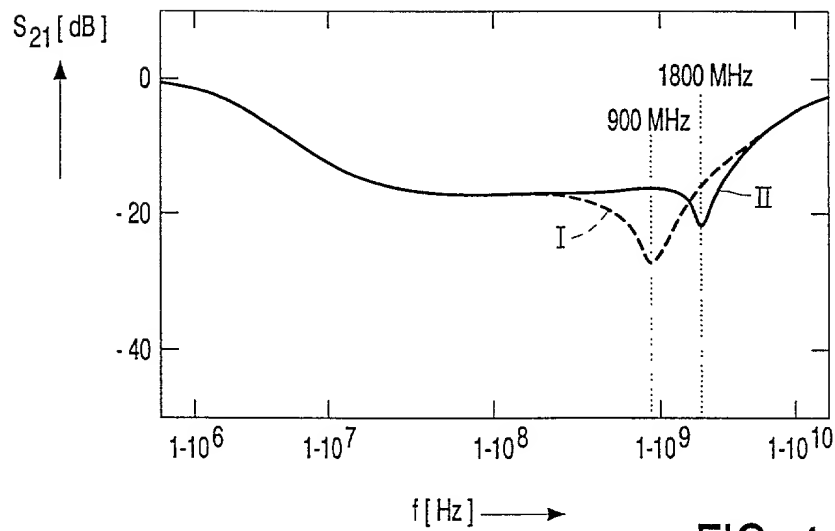


FIG. 4

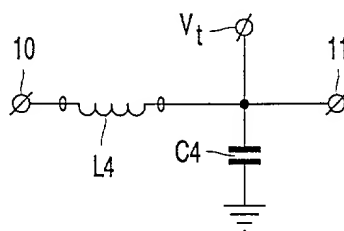


FIG. 5

DECLARATION and POWER OF ATTORNEY

ATTORNEY'S DOCKET NO.:
PHD 99.046 US

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

"Voltage-dependent thin-film capacitor"

the specification of which (check one)

☐ is attached hereto.

☐ was filed on _____ as Application Serial No. _____ and was amended on _____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by the amendment(s) referred to above.

I acknowledge the duty to disclose information which is material to patentability of this application in accordance with Title 37, Code of Federal Regulations, §1.56(a).

I hereby claim foreign priority benefits under Title 35, United States Code, § 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

PRIOR FOREIGN APPLICATION(S)

COUNTRY	APP. NUMBER	DATE OF FILING (DATE, MONTH, YEAR)	PRIORITY CLAIMED UNDER 35 U.S.C. 119
Germany	19915247.0	3 April 1999	YES

I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35 United States Code, §112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, §1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

PRIOR UNITED STATES APPLICATION(S)

APPLICATION SERIAL NUMBER	FILING DATE	STATUS (PATENTED, PENDING, ABANDONED)

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith. (list name and registration number)

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of

Atty. Docket

MAREIKE KLEE ET AL

PHD 99,046

Serial No.

Group Art Unit

Filed: CONCURRENTLY

Ex.

VOLTAGE-DEPENDENT THIN-FILM CAPACITOR

Honorable Commissioner of Patents and Trademarks
Washington, D.C. 20231

APPOINTMENT OF ASSOCIATES

Sir:

The undersigned Attorney of Record hereby revokes all prior appointments (if any) of Associate Attorney(s) or Agent(s) in the above-captioned case and appoints:

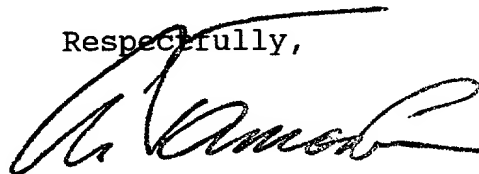
NORMAN N. SPAIN

(Registration No. 17,846)

c/o U.S. PHILIPS CORPORATION, Intellectual Property Department, 580 White Plains Road, Tarrytown, New York 10591, his Associate Attorney(s)/Agent(s) with all the usual powers to prosecute the above-identified application and any division or continuation thereof, to make alterations and amendments therein, and to transact all business in the Patent and Trademark Office connected therewith.

ALL CORRESPONDENCE CONCERNING THIS APPLICATION AND THE LETTERS PATENT WHEN GRANTED SHOULD BE ADDRESSED TO THE UNDERSIGNED ATTORNEY OF RECORD.

Respectfully,



Algy Tamoshunas, Reg. 27,677
Attorney of Record

Dated at Tarrytown, New York
this 28TH day of MARCH, 2000.